Notice of Allowability	Application No. 10/604,354	Applicant(s) CHENG, ET AL.	
	Examiner Luis Roman	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/19/06*.

2. ☒ The allowed claim(s) is/are *1,6,10-12,14,15 and 19-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Examiner Amendments

Examiner acknowledges a submission of the amendment filled on 10/19/2006. Claims 10-12 have been kept original, claims 1, 6 have been amended, claims 14 & 15 have been kept as previously presented and claims 2-5, 7-9, 13, and 16-18 have been cancelled. Claims 19-21 have been added.

Claim 19 (new) the electrostatic discharge protection circuit of claim 14 wherein the input end of the npn Darlington circuit is connected to an input end of another circuit.

Claim 20 (new) the electrostatic discharge protection circuit of claim 14 wherein the input end of the npn Darlington circuit is connected to a voltage source.

Claim 21 (new) the electrostatic discharge protection circuit of claim 14 further comprising: a pnp Darlington circuit, an input end of the pnp Darlington circuit connected to the input end of the npn Darlington circuit, an output end of the pnp Darlington circuit connected to a voltage source; and a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the PMOS transistor connected to the input end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp Darlington circuit, a gate of the PMOS transistor connected to the output end of the pnp Darlington circuit.

Reasons for allowance

The following is an examiner's statement of reasons for allowance.

Regarding claim 1: The closest references are:

- "Substrate-Triggering Electrostatic Discharge Protection Circuit For Deep-Submicron Integrated Circuits"
  Ker et al. (US 6072219)
  issued on June 06, 2000.
- "Electrostatic Discharge Power Clamp Circuit"
  Voldman et al (US 6549061)
  issued on April 15, 2003.
- "BIMOS Current Driver Circuit"
  Glica et al. (US 5262689)
  issued November 16, 1993
- "Isolated DMOS IC Technology"
  Williams et al. (US 5485027)
  issued January 16, 1996.

These patents disclose:

- Ker et al.'219: an electrostatic discharge (ESD) protection circuit (Abstract) comprising an N-type channel metal-oxide transistor (N-MOS) (Col. 5 lines 37-53 & Fig. 4 element N1), a drain of the NMOS transistor connected to a clamp circuit (Fig. 4 elements B1, F1), a source of the NMOS transistor connected to a control end of the transistor circuit (Fig. 4 elements B1, F1) and a gate of the NMOS transistor connected to the output end of the transistor circuit (Fig. 4 element V_{SS}).
- Voldman et al.'061: a clamp circuit comprising a NPN Darlington circuit (Fig. 6 element 604), with an input end (Fig. 6 element 210), an output end

(Fig. 6 element 212) and the output end of the NPN Darlington being grounded (Fig. 6 element 212).

- Glica et al.'689: an NPN Darlington circuit comprising two NPN-type bipolar junction transistors (BJT) (a Darlington consists of two transistors equally constructed connected in tandem configuration), each NPN BJT comprising an N+ buried layer (Fig. 3B), a P well formed on the N+ buried layer (Fig. 3B), a N well formed on the N+ buried layer around the P well (Fig. 3B element NBODY) and an N+ node formed in a top side of the P well (Fig. 3B element N+).
- Williams et al.'027: an NMOS transistor comprising a N+ buried layer (Fig. 22 element 123), a P well formed on the N+ buried layer (Fig. 22 element 201), an N well formed on the N+ buried layer around the P well (Fig. 22 element 203) and two N+ nodes (Fig. 22 elements 211, 213) formed in a top side of the P well.

These patents do not disclose:

- A P-epi layer formed on the P-substrate and wherein the N wells of the two NPN BJT's and the NMOS transistors are formed on the P-epi layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Patent Examiner
Art Unit 2836

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These patents do not disclose:

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LR/110106

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